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JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
PASADENA, CALIFORNIA

Rgd 29528

RE-ORDER NO. 63-800

FIRST QUARTERLY REPORT
ON
MOLECULAR POWER SUPPLY SYNCHRONIZER
FOR THE PERIOD
MAY through JULY, 1962

This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, sponsored by the National Aeronautics and Space Administration under Contract NAS7-100.

JPL ORDER 950237
under
NAS 7-100

Westinghouse Electric Corporation
Astroelectronics Department
Newbury Park California

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LIST OF ILLUSTRATIONS

CONTRACT OBJECTIVES

The prime objective of this contract is to prove the feasibility of forming an entire subsystem on a single silicon slice or on as few chips as possible. The subsystem chosen for the program is the digital portion of a power supply synchronizer. The input to the synchronizer is a 38.4 KC square wave of 3 to 5V peak to peak, capable of switching 3ma. The synchronizer will have four outputs: number one will be a 2.4 KC square wave at a normal amplitude of 5.5V peak to peak capable of switching a 10ma current; numbers two, three and four will be the three phases of a three phase 400 cycle square wave and are to be capable of switching a 50V peak to peak signal to an 8.2K load from a 52V power supply.

This program is a joint effort, in that portions of the actual design as well as new techniques which are proprietary in nature are being funded by Westinghouse. JPL is supporting the effort to adapt the designs and techniques to their specific application.

GENERAL APPROACH

The approach to the problem is to form the simplest possible logic configuration which can reliably produce the desired signals from a single type of logic circuit, in this case a NAND gate, and to form these with the necessary interconnecting patterns on a single silicon wafer. For dissipation reasons this wafer will be run from a low voltage power supply. A second and much smaller slice will have the three phase output switches formed on it and will be operated from the 52V power supply. Logic gates of the type required are now being fabricated on a pilot line. These devices are formed on a 7/8" diameter silicon wafer, a portion of which, measuring .55" x .4", contains enough gates to perform the logic required. The remaining area to make a square .55" x .55" will be used to mount the chip or chips containing the three phase output switches.

PROJECT BREAKDOWN

The project has been subdivided into the following sub projects:

(a) Logic design and confirmation.

(b) Interconnection pattern design.

(c) Interconnection method design and development.

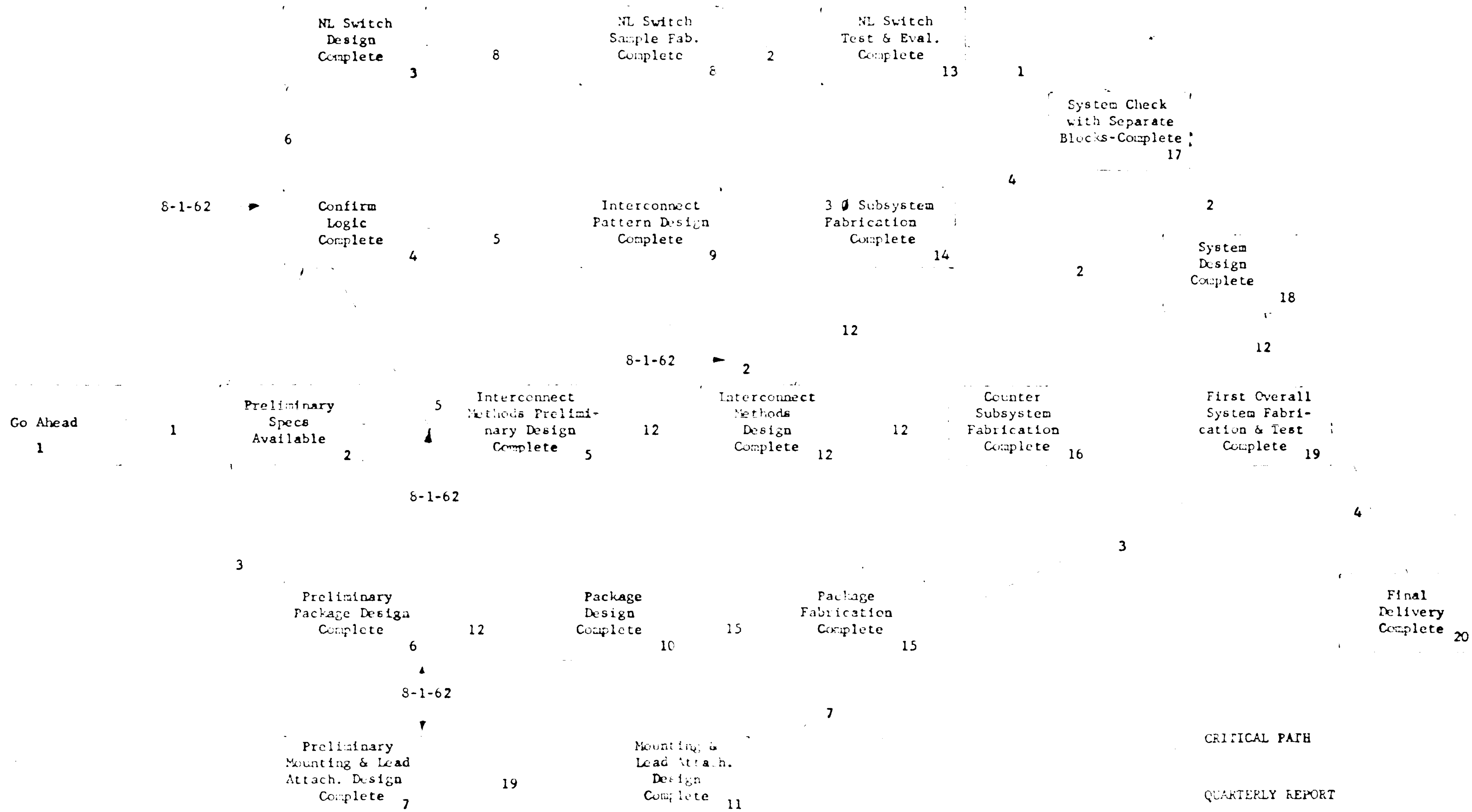
(d) Output switch (called non-linear load switch) electrical and device design.

(e) Packaging design.

(f) Partial system fabrication.

(g) Overall system fabrication.

The PERT diagram in Figure 1 shows these areas and time estimates as of 1 August, 1962. Figure 2 is a tabulation of path lengths from this chart.



CRITICAL PATH

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FIGURE 1

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TABULATION OF PERT CHART PATHS

to 8-1-62	11	to 8-1-62	11	to 8-1-62	11	to 8-1-62	11	to 8-1-62	11	to 8-1-62	11	to 8-1-62	11
8-1-62 to3	6	8-1-62-12	2	8-1-62-5	5	8-1-62-10	12	8-1-62-11	19	8-11-62-12	2	8-1-62-5	55
3 - 8	8	12 - 14	12	5 - 12	12	10 - 15	15	11 - 15	7	12 - 16	12	5-12-62	12
8 - 13	2	14 - 17	4	12 - 14	12	15 - 19	3	15 - 19	3	16 - 17	2	12 -16-	12
13- 17	1	17 - 18	2	14 - 17	4	19 - 20	4	19 - 20	4	17 - 18	2	16 - 17	2
17- 18	2	18 - 19	12	17 - 18	2					18 - 19	12	17 - 18	2
18- 19	12	19 - 20	4	18 - 19	12					19 - 20	4	18 - 19	12
19- 20	4			19 - 20	4							19 - 20	4
WEEKS	46		47		62		45		44		45		60

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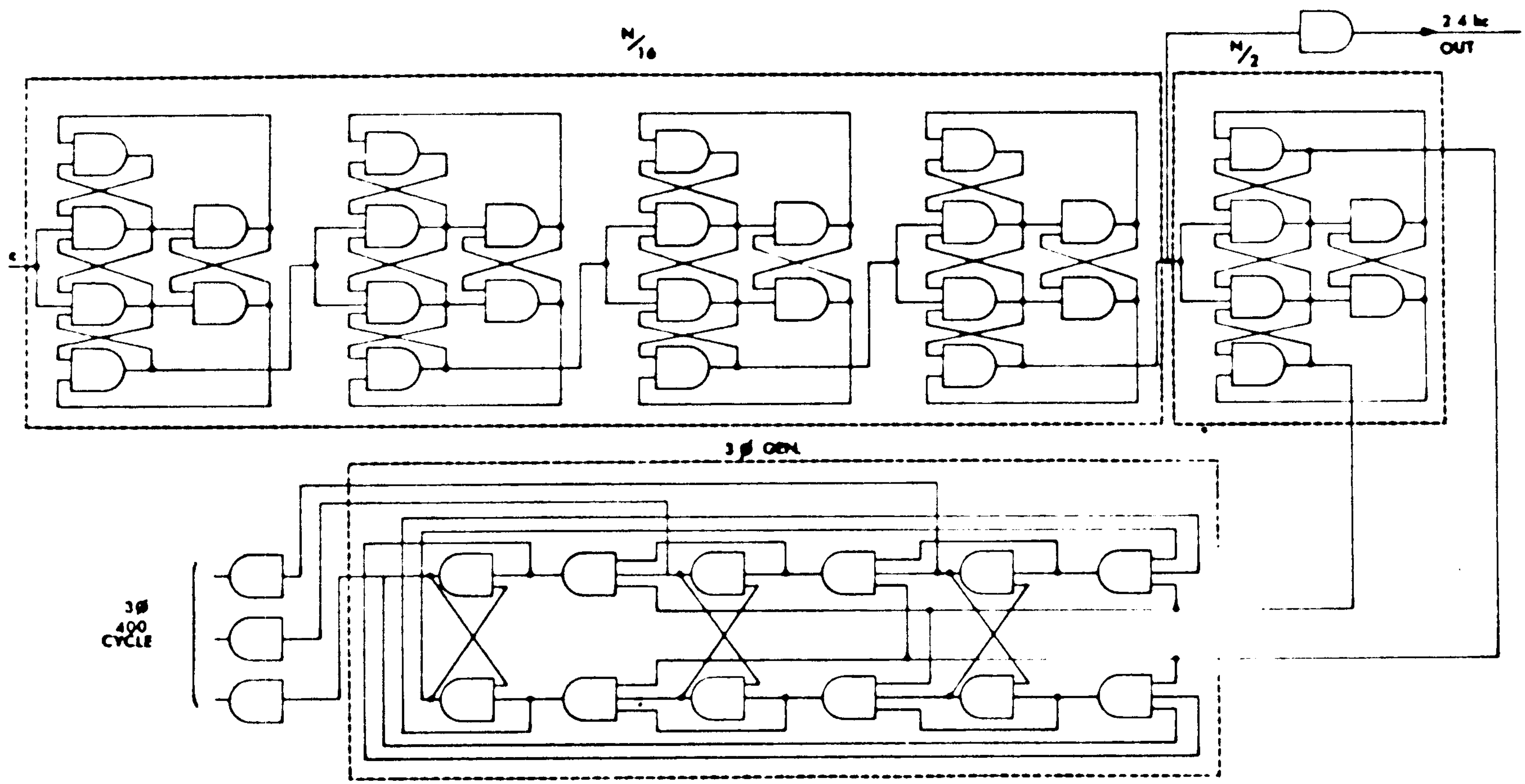
FIG. 2

LOGIC DESIGN

The final logic design is shown in Figure 3 and consists of five stages of D.C. coupled binary counters, each stage using six NAND gates, a three phase generator using twelve NAND gates, an output buffer using a single NAND gate and the three high voltage output switches which are a PNP-NPN combination.

This entire logic arrangement has been breadboarded using conventional components and the portions (all except the output switches) formed with NAND gates have been assembled with Westinghouse planar double NAND gates. A picture of the latter system is shown in Figure 4 and wave forms from the 2.4 KC and the three phase outputs as presented on a four trace oscilliscope are shown in Figure 5.

OVER ALL LOGIC DESIGN



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INTERCONNECTION PATTERN DESIGNS

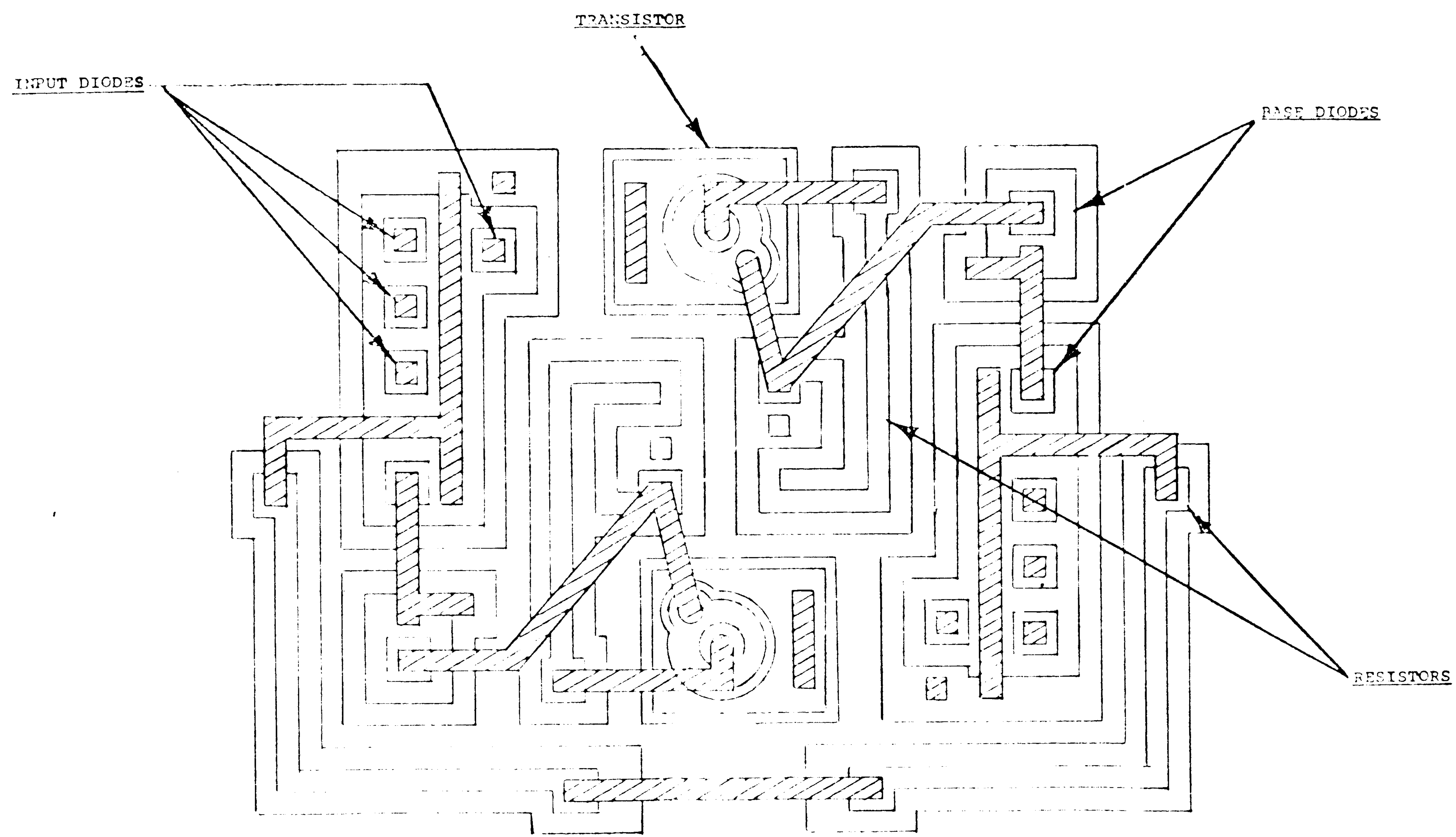
Interconnecting the NAND gates on a single wafer will be accomplished by evaporating aluminum patterns. Designing these patterns is similar to designing printed circuit patterns with some added restrictions in routing and with cross-over points being limited to certain specific places on the wafer.

The present design consists of four diffused cross-over patterns associated with each double NAND gate pattern located in the area between the gates. (See Figure 6).

A basic interconnection pattern has been designed which forms a D.C. coupled binary counter from three double NAND gates (see Figure 8). The logic for this pattern is shown in Figure 7.

It will be noted that the three double NAND gates used are located one above the other and the input to the counter and output from the counter are so located that putting down identical patterns on adjacent rows connects the binary counters together. This will permit the N/16 counter pattern masks to be made with a conventional step and repeat camera setup.

The logic for the three phase generator and the pattern to form this logic is shown in Figures 9 and 10. This logic is formed on a strip of double NAND gates, two rows high by four rows long, and is so arranged that it can be placed directly below the four rows which form the N/16 counters. The N/2 counter and output buffer gate for the 2.4 KC will be formed in an additional column to the right of N/16 and three phase generator. In the final arrangement, the three sets of patterns will be formed into a single mask, and all interconnections necessary for forming the complete synchronizer logic will be made in one operation.



DOUBLE NAND
GATE PATTERN

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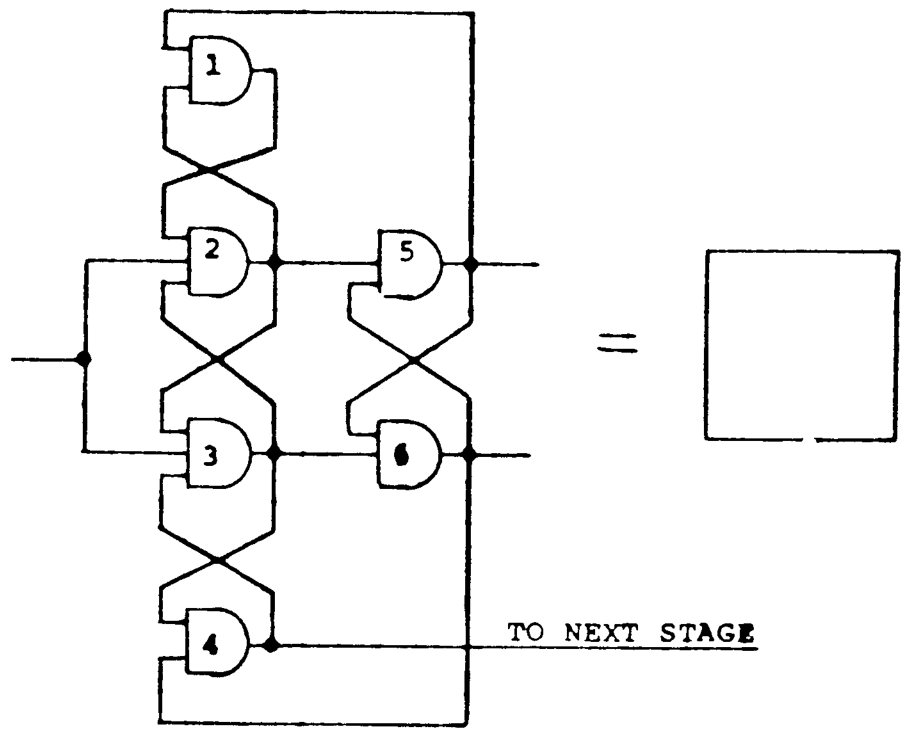
Figure 6

D. C. COUPLED BINARY COUNTER

INPUT



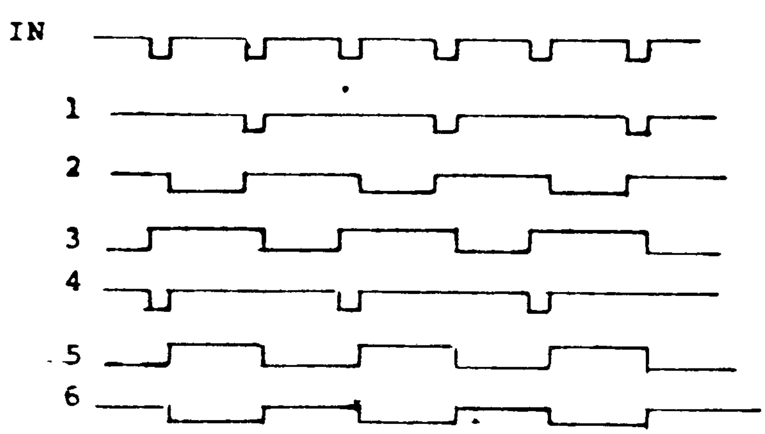


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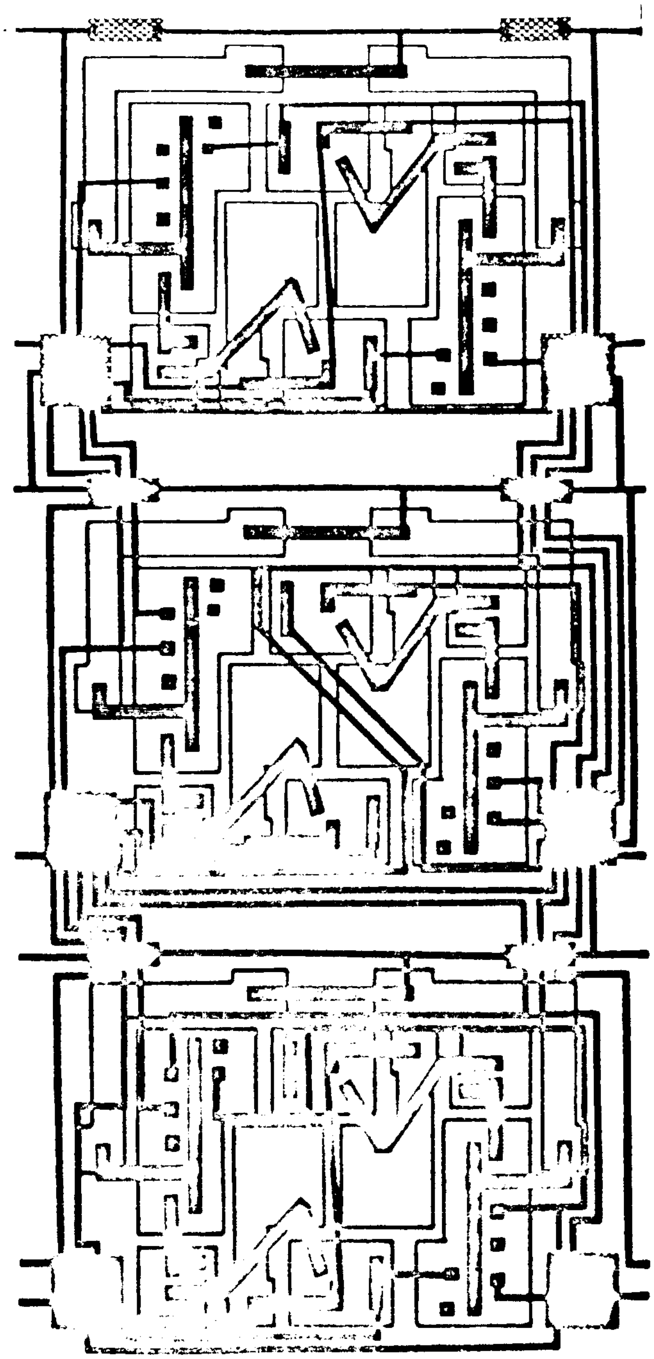
FIG. 7

BINARY COUNTER
INTERCONNECT PATTERN



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THREE PHASE GENERATOR LOGIC

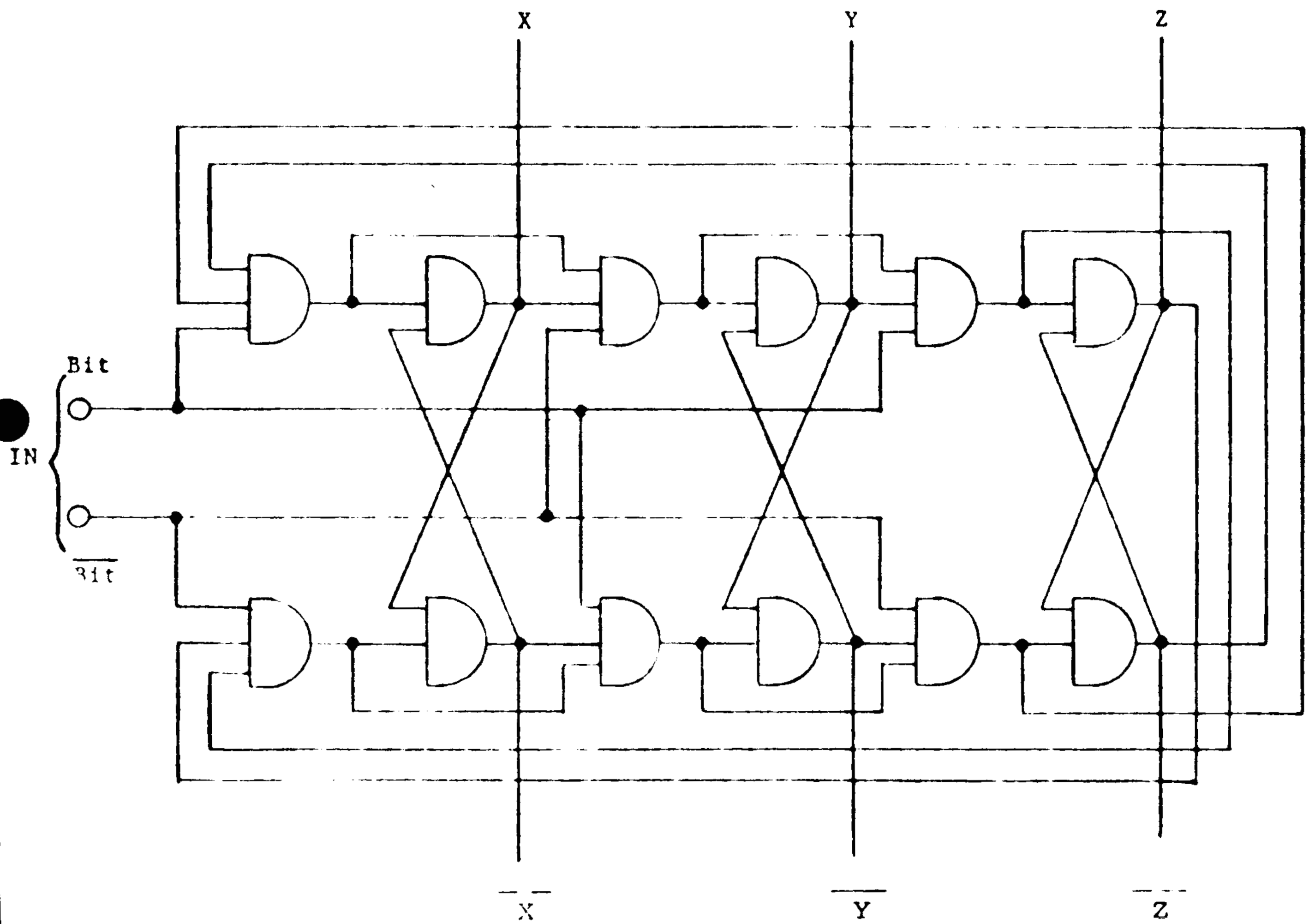

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FIG. 9

GENERATOR LOGIC PATTERN

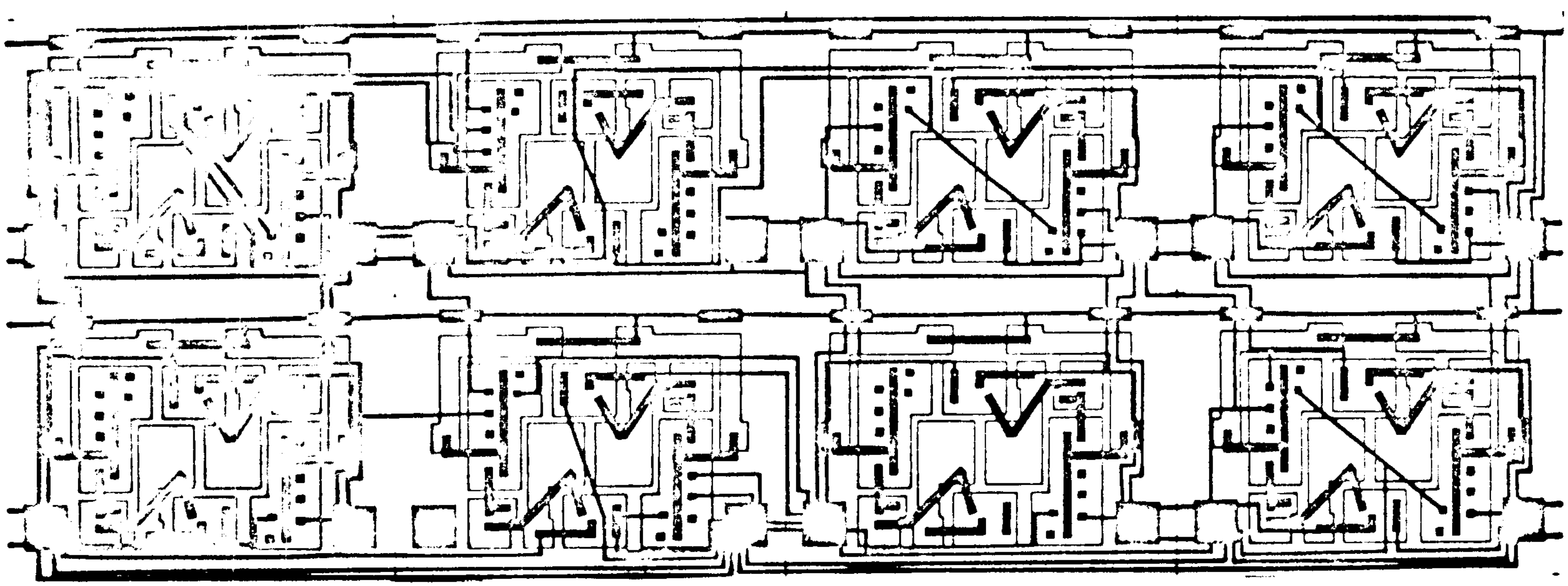

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FIG. 10

INTERCONNECTION METHOD DESIGN

Initial studies of the logic indicated that cross-overs would be required in the interconnection pattern. For this reason, experiments were performed to determine the impedance of diffused under connections. This is accomplished by diffusing a high concentration impurity into the substrate at the intersection. This can be performed with the emitter formation process. Sheet resistances of 1.5 ohms per square were obtained after some improvements in processing were made. It is expected that, by further refinement, .5 ohms per square can be obtained. This value should permit connection of the two layers, aluminum top and diffused bottom, with an oxide insulation between. Tests show that isolation of greater than 200 volts is present on good units. Capacitance measurements have not been made to date, but are not expected to cause a problem at the current operating speeds.

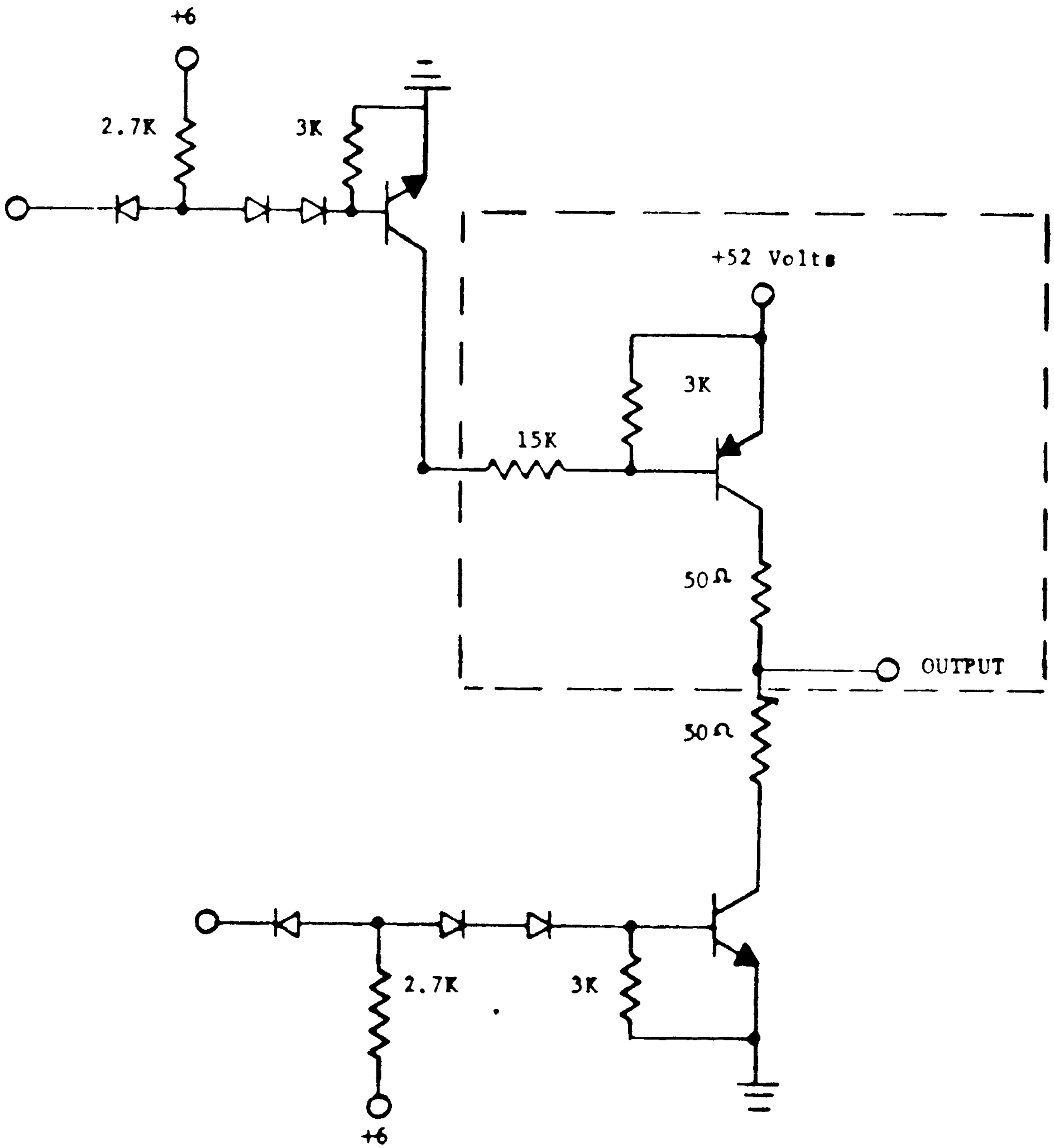
Due to the complexity of the connection pattern it would be extremely desirable to be able to ground each circuit to the substrate directly for a ground return. However, with the current substrate material an impedance in the order of 1 kilo ohm would result, which of course is intolerable.

A method for providing adequate resistivity for device parameters yet lowering the impedance by orders of magnitude is being investigated. Essentially this involves growing an epitaxial layer on a low resistivity substrate.

NON-LINEAR LOAD SWITCH

Initial design consideration indicated that the 50 volt square wave output switches could be made by using an NPN switching transistor with a field effect load resistor. This device would limit the current flow in the "on" condition and allow the output to approach the 52 volt supply in the "off" condition. However, in order to obtain a triode region resistance of small enough value to meet the 50$\pm$ 1 volt output requirement, pinch off current greater than 15 milliamps would be dictated due to the physical limitations of the device structure. This would result in a power dissipation of greater than .37 watts per output switch, an intolerable situation for this application. For this reason, a circuit with a "switching load" was designed for performing the high voltage output. This circuit shown in Figure 11, provides low power dissipation because a negligible current flows during the ground portion of the cycle. The necessity of both NPN and PNP structures greatly complicates the processing for producing a single chip. For reasons of increased reliability and to decrease the complexity of processing, the decision was made to fabricate the switch in two separate operations. The dotted lines on Figure 11 indicate the portions as divided. These devices will be realized by a combination of epitaxial and diffusion techniques. During the past period, the output circuit has been designed and breadboard tested.

The preliminary solid state design has been completed and fabrication tests have been started.



NON LINEAR LOAD SWITCH SCHEMATIC

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FIG. 11

PACKAGE AND DIE ATTACH DESIGN

A package similar to that shown in Figure 12 has been proposed. The main feature of this design is the hard brazed tungsten substrate, to which the chip will be alloyed. In this way we hope to provide a thermal match and at the same time provide a very excellent heat sink. The design of experimental headers for this package is complete and materials are on order. The design of the jigs for fusing the header is also complete and the jigs are on order. Lead material, glass preforms gold plated kovar and cut to size tungsten have been received and the tungsten has been sent out for gold plating and gold silicon cladding. The die attach platform is being designed. When all material and jigs are available, sample packages will be assembled with dummy dice and these will be evaluated for their ability to meet the environmental specifications.

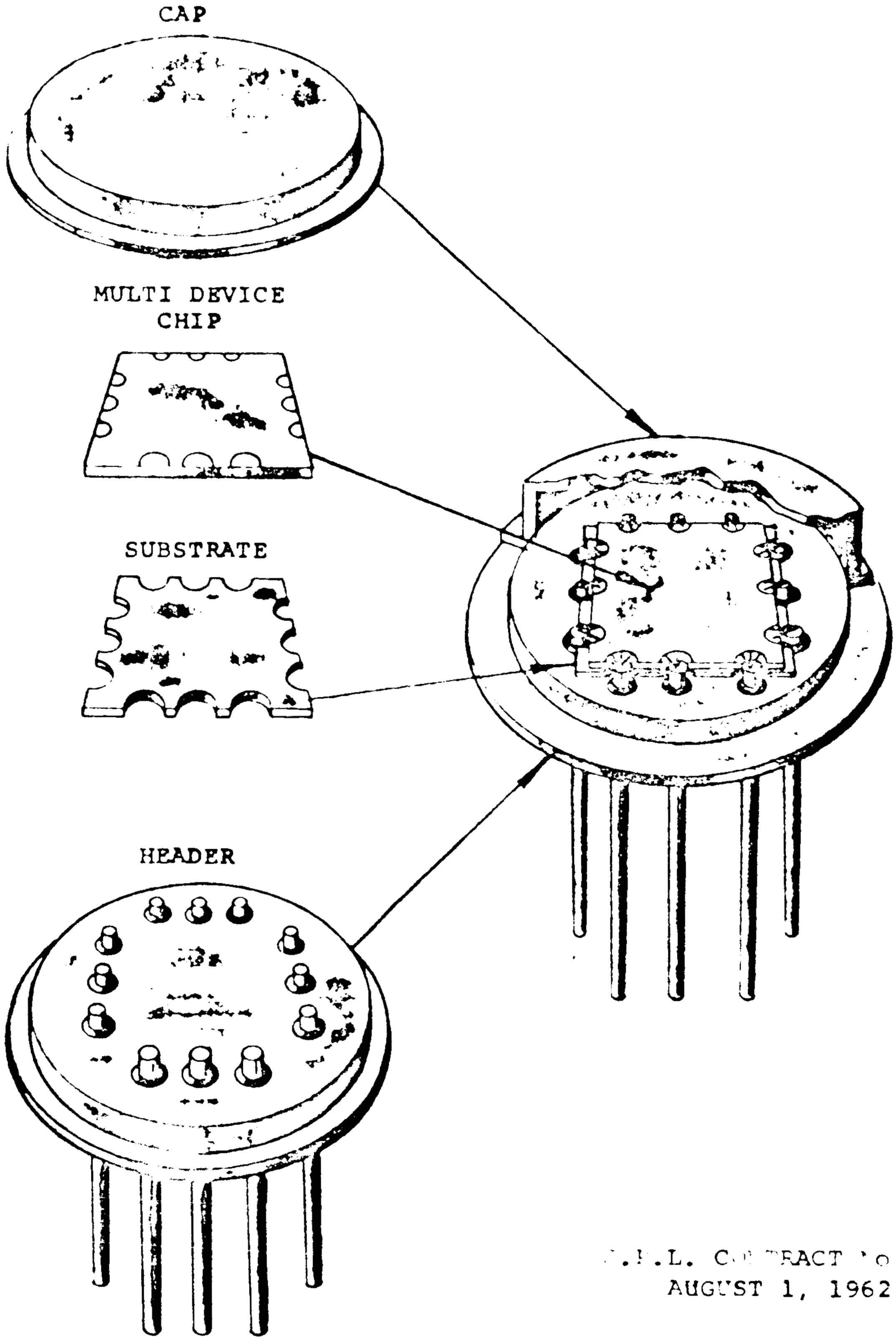

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FIG. 12

PRELIMINARY PACKAGE DESIGN